In the Claims:

Please amend the claims as follows:

1. (amended) A partially fabricated wafer, comprising:

at least one probe pad;

multiple test structures which are selectably multiplexed to said probe pad in dependence on a voltage applied thereto.

4. (amended) The wafer of Claim 1, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a sequence of voltages applied to said probe pad.

5. (amended) A partially fabricated wafer including die separated by scribelines, comprising:

at least one probe pad in a scribeline;

multiple test structures in said scribeline which are all physically close to said probe pad, and which are selectably multiplexed to said probe pad in dependence on at least one global input.

6. (amended) The wafer of Claim 5, wherein said probe pad occupies more than half the width of said scribeline.

7. (amended) The wafer of Claim 5, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a voltage applied to said probe pad.

8. (amended) The wafer of Claim 5, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a sequence of voltages applied to said probe pad.

9. (amended) A scribeline test circuit, comprising:

a test selector circuit located in a single scribeline portion between two adjacent die locations;

multiple test structures, also located in said single scribeline portion; and

at least one probe pad, also located in said single scribeline portion;

wherein said test selector circuit makes an electrical connection from said probe pad only to a selected one of said test structures, in dependence on a voltage applied at said probe pad.

11. (amended) The circuit of Claim 9, wherein said multiple test structures are selectively multiplexed to said probe pad in dependence on a sequence of voltages applied to said probe pad.

12. (amended) A method for characterizing integrated circuits using multiple test structures, comprising the steps of:

(a.) applying a selection signal to a probe pad coupled to said multiple test structures, to drive a selector circuit to connect a selected one of said multiple test structures to said pad; and

(b.) applying a controlled voltage to said pad, and thereby measuring the electrical characteristics of the selected one of said multiple test structures.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1-12 were pending in this application. Claims 1, 4, 5, 6, 7, 8, 9, 11, and 12 have been amended to better define the scope of the claimed invention.